

*Lab Information*

## Digital Logic Design Notes

*Lab Requirements and Assignments*

Revision 1  
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*Lab Requirements and Assignments*

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**Required Lab Write-up Format**

The following format must be used for all lab write-ups:

Lab #, Lab Title  
Date

**Problem**

State the problem to be solved or task to be accomplished. If you can simplify the problem from the form in which it was originally stated by weeding out the red herrings, feel free to do so.

**Procedure**

State how you approached the problem, i.e., you started by writing the equations, you drew the logic diagram first, you copied it from a classmate, etc. Be sure to include truth tables, maps, and function equations where appropriate or asked for.

**Results**

Describe your findings and conclusions. Discuss alternate ways of solving the problem if you can think of any. As appropriate, this section should include equations, equation simplification procedures, and logic diagrams of all circuits used. Be sure to label all input and output logic signals and include the IC part numbers and pin numbers. Your logic diagram should be complete enough that your circuit can be reconstructed from it.

You do not have to use a computer program to generate your logic diagrams but they must be drawn neatly using a straight edge. A 1/2 or 3/4 scale standard logic symbol template is also highly recommended and may be purchased from many electronics or drafting supply stores. **ANY DRAWINGS I CONSIDER TO BE SUBSTANDARD WILL BE REJECTED.**

**Parts List**

List all parts by the most complete part number available including the manufacturer, quantity, and your own series designator. A technician or manufacturing company may need to order the parts.

**Opinions and Conclusions**

Was the lab worthwhile, too hard, too easy, redundant, unclear, wonderful, etc.



## Sample Lab Problem

### Digital Logic Design Sample Lab Problem

A certain laboratory rat has been trained to step on various switches in its cage to get food and water. There are five switches. One switch delivers nuts, a second delivers corn, a third delivers water, and a fourth delivers all three. In order for any of these switches to work, however, the rat must hold the fifth switch activated when activating any of the other four. If the rat is able, it may activate more than one of the food and water switches at a time to get the combinations associated with those switches.

Using LEDs to represent the water and food types and DIP switches to represent the cage switches, design and build a logic circuit which will demonstrate a solution to this problem.

## Sample Lab Problem Solution

Digital Logic Design Sample Lab Problem Write-up  
Laboratory Rat Food Problem  
July 17, 1985

### Simplified Problem

There are five switches. One switch represents nuts, a second represents corn, a third represents water, and a fourth represents all three. In order for any of these switches to work, however, a fifth switch must be activated when activating any of the other four. More than one of the first three switches may be activated at one time to get the combinations associated with those switches.

Using LEDs to represent the water and food types, design and build a logic circuit which will demonstrate a solution to this problem.

### Procedure

Because it was not specifically stated whether an LED should be on or off when a particular food is selected, I have arbitrarily chosen to have the on state represent selection and the off state to represent non-selection for all LEDs. Similarly, it was not stated whether a switch is open (off) or closed (on) when activated. I have chosen the closed (on) state to represent the activated condition for all switches except the ENABLE.

Refer to logic diagram figure 1 which represents the solution to the problem along with the equations. Because of the way the DIP switches are used, the closed (on) state represents a logic low (logic 0). Because of the way the LEDs are connected, their on state also represents a logic low (logic 0).

The truth table is as follows (continued on next page):

Laboratory Rat Food Problem Truth Table								
min	A	B	C	D	E	F	G	H
m0	0	0	0	0	0	1	1	1
m1	0	0	0	0	1	0	0	0
m2	0	0	0	1	0	1	1	1
m3	0	0	0	1	1	0	0	0
m4	0	0	1	0	0	1	1	1
m5	0	0	1	0	1	0	0	0
m6	0	0	1	1	0	1	1	1
m7	0	0	1	1	1	0	0	1
m8	0	1	0	0	0	1	1	1
m9	0	1	0	0	1	0	0	0
m10	0	1	0	1	0	1	1	1
m11	0	1	0	1	1	0	1	0
m12	0	1	1	0	0	1	1	1
m13	0	1	1	0	1	0	0	0
m14	0	1	1	1	0	1	1	1
m15	0	1	1	1	1	0	1	1
m16	1	0	0	0	0	1	1	1
m17	1	0	0	0	1	0	0	0
m18	1	0	0	1	0	1	1	1
m19	1	0	0	1	1	1	0	0
m20	1	0	1	0	0	1	1	1
m21	1	0	1	0	1	0	0	0
m22	1	0	1	1	0	1	1	1
m23	1	0	1	1	1	1	0	1
m24	1	1	0	0	0	1	1	1
m25	1	1	0	0	1	0	0	0
m26	1	1	0	1	0	1	1	1
m27	1	1	0	1	1	1	1	0
m28	1	1	1	0	0	1	1	1
m29	1	1	1	0	1	0	0	0
m30	1	1	1	1	0	1	1	1
m31	1	1	1	1	1	1	1	1

A = 0 => NUT switch activated

B = 0 => CORN switch activated

C = 0 => WATER switch activated

D = 0 => ALL switch activated

E = 1 => ENABLE switch activated

F = 0 => Give NUTS - LED on

G = 0 => Give CORN - LED on

H = 0 => Give WATER - LED on

(NOTE: A legend describing the meaning of the 1s and 0s in the truth table must be provided adjacent to the truth table as shown here. Putting this information only on a different page is not acceptable.)

**Initial Equations**

Because there are fewer 0s than 1s in each output, I chose to write the equations for F', G', and H' and complement back to F, G, and H after simplification.

$$F' = m1 + m3 + m5 + m7 + m9 + m11 + m13 + m15 + m17 + m21 + m25 + m29$$

$$G' = m1 + m3 + m5 + m7 + m9 + m13 + m17 + m19 + m21 + m23 + m25 + m29$$

$$H' = m1 + m3 + m5 + m9 + m11 + m13 + m17 + m19 + m21 + m25 + m27 + m29$$

(NOTE: If these equations differ from the ones actually used to build your circuit, you must show all steps used to get to the final equations. This should consist of the math steps, the Karnaugh maps with groupings, etc.)

**Final Simplified Equations**

$$F' = (A' + D')E \quad F = AD + E'$$

$$G' = (B' + D')E \quad G = BD + E'$$

$$H' = (C' + D')E \quad H = CD + E'$$

**Results**

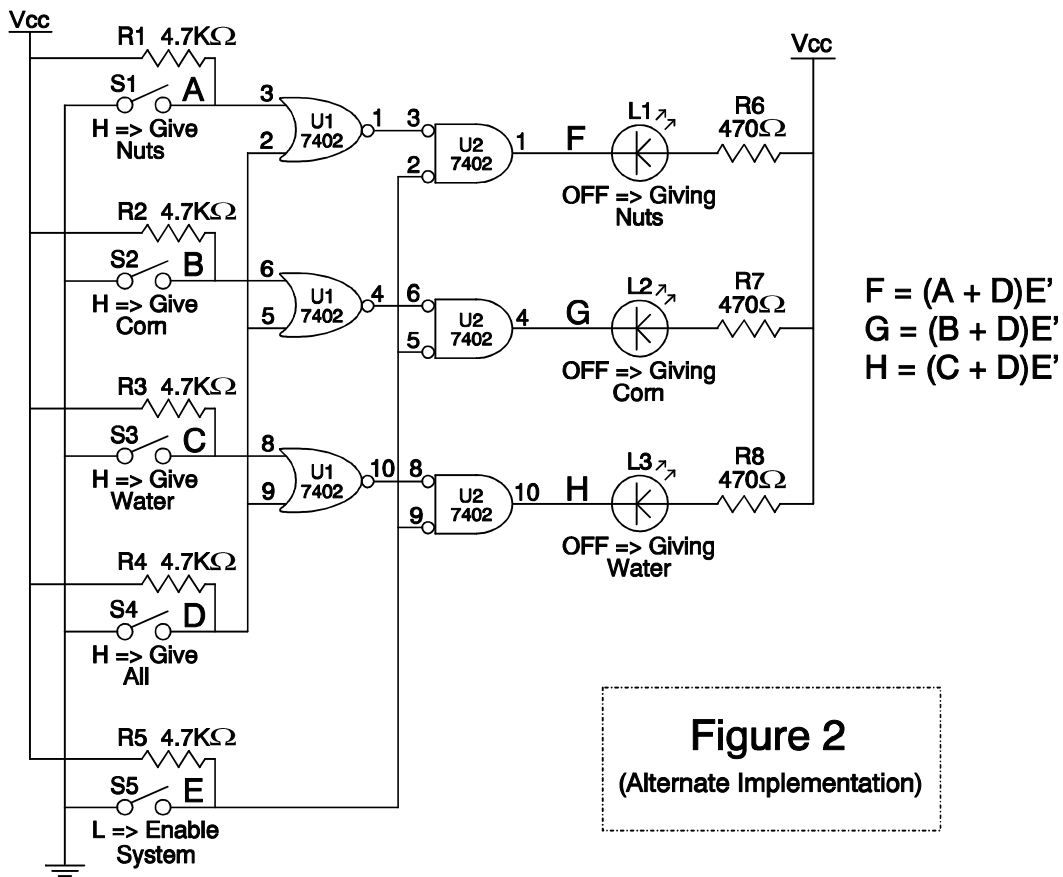
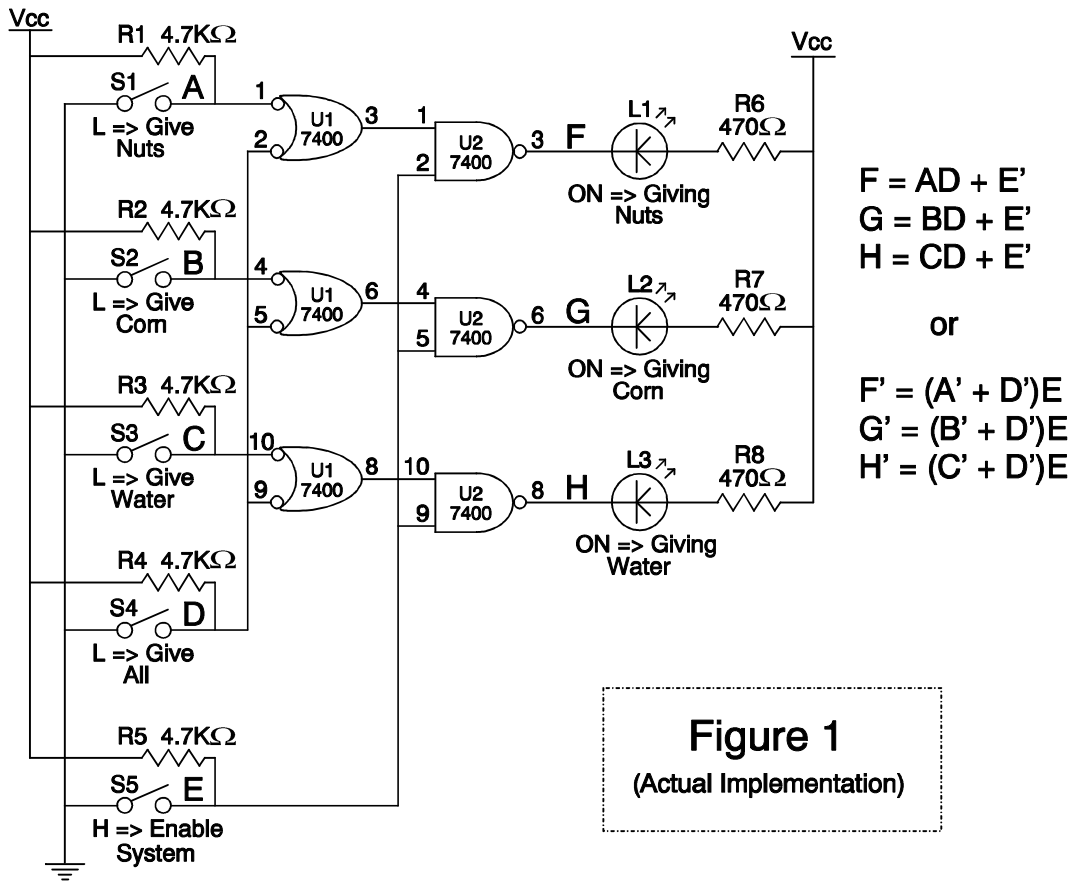
The circuit worked like a charm on only the 50th rewiring job. Figure 1 is the circuit actually used. An alternate circuit is shown in figure 2. Figure 2 reverses my assumptions about the state of the LEDs when selected and the state of the switches when activated. Other circuits with various combinations of these assumptions are possible although possibly not very practical.

**Parts List**

U1,U2: Integrated Circuit, SN74LS00N, Texas Instruments	2ea.
L1-L3: LED, red, 16ma. @ 1.5v, Monsanto	1ea.
S(1-5): DIP switch, 16 pin, Amp Inc.	1ea.
R1-R5: Resistor, 4.7K ohm, 1/4 watt, CB 472, Allen-Bradley	5ea.
R6-R7: Resistor, 470 ohm, 1/4 watt, CB 4715, Allen-Bradley	3ea.
Vcc: Power Supply, 5v @ 1a, EM5/6B, Powerco	1ea.
Prototype Board, Radio Shack	1ea.
Hookup wire, 22ga.	3ft.

**Opinions and Conclusions**

This lab was a total waste of time. After I finally did get the circuit operating, the rat couldn't operate the DIP switches and ended up electrocuting itself.



**Lab #1**  
(50 points)

Part 1: (40 points)

Target IC / GATE count: .75 / 3

As a digital designer you have been asked to design an alarm system. The alarm monitors one door and one window. It has an enable switch and a panic button and sounds whenever:

- A. the system is enabled and either the door or the window is open or,
- B. the panic button is pressed (regardless of the state of the enable switch).

Represent each of the door, the window, the enable switch, and the panic button by a separate switch on the DIP switch and the alarm by an LED (light emitting diode). Design, document, construct, and demonstrate a working system.

Part 2: (10 points)

No hardware construction is required for this part, which may be turned in anytime up through the last class meeting. You may assume the pinout of a 74HC00 to be the same as that of a 74ALS00.

Using the concepts covered in class concerning mixing logic families, design and document an interface for a 74ALS03 driving one input of a 74HC00. Satisfy yourself and me that this same interface would work if the 74ALS03 were replaced by a 74ALS04.

Similarly, design and document an interface for a 74HC00 driving a 74ALS04 input.

For both interfaces, list what the minimum logic HIGH and maximum logic LOW voltages would be on the interface line connecting the two gates.

**Lab #2**  
(50 points)

Target IC / GATE count: 2 / 5

The republic of Freedonia has a three member legislature (A, B, C) and a president (P). Legislation becomes law:

- (1) if there is a majority "yes" vote of the legislature and there is no presidential veto or,
- (2) if there is a unanimous "yes" vote of the legislature (regardless of a presidential veto).

You have been hired to design a voting display that:

- A. displays the vote of each member of the legislature,
- B. displays whether or not the president is casting a veto and,
- C. displays whether or not the legislation becomes law.

You may either assume that the president can cast a veto at any time or that a veto may be cast only if two of the three members are voting for the legislation. Don't care states should be examined to see if they can simplify the implementation.

Use switches to cast the votes/veto and use LEDs for the displays. Develop the Boolean function and minimize it using the Karnaugh Map method. Design, document, construct, and demonstrate a working system. Implement it using either a two-level NAND or a two-level NOR configuration and no inverters.

**Lab #3**  
(50 points)

Part 1: (25 points)

Target IC / GATE count: 1 / MSI

Redesign, build, debug, and document the voting display of lab #2 using the multiplexer method for implementing Boolean functions. Include a truth table and the equation for the function. Also include the mechanical "minterm table" used to develop the function.

Part 2: (25 points)

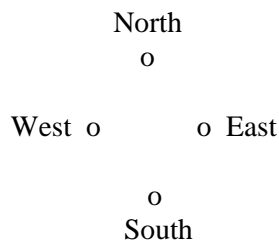
Target IC / GATE count: 3 / 4+MSI

Design, build, debug, and document a digital weather vane to the following specifications:

- a. The shaft of the vane shall have a mechanical encoding system attached to it which produces the following direction codes:

Weather Vane Direction Codes	
DIRECTION	CODE
North	000
Northeast	001
East	011
Southeast	010
South	110
Southwest	111
West	101
Northwest	100

- b. The direction display shall consist of four LEDs arranged in a diamond pattern as shown below:



- c. Whenever the encoding system indicates one of the four primary directions (North, East, South, or West), the corresponding LED shall be on and the other three shall be off. Whenever one of the secondary directions (NE, SE, SW, or NW) is indicated, the two adjacent LEDs corresponding to the direction shall be on and the other two shall be off.

Use the decoder method to implement the design, using a 74LS138 and NAND gates. Use three switches on the DIP switch to input the three bit codes for the eight directions. Include a truth table and the equation for each function.

**Lab #4**  
(50 points)

Target IC count: 6 ICs

You have been hired by an automobile manufacturer to design a sequential turn signal for a tail light system. The left and right tail lights each consist of three lamps as shown below:

<b>L1</b>	<b>L2</b>	<b>L3</b>		<b>R3</b>	<b>R2</b>	<b>R1</b>
-----------	-----------	-----------	--	-----------	-----------	-----------

Whenever one of the turn signal switches is on the following lamp sequences are displayed repeatedly:

Left Signal			Right Signal		
<b>L1</b>	<b>L2</b>	<b>L3</b>	<b>R3</b>	<b>R2</b>	<b>R1</b>
off	off	on	on	off	off
off	on	on	on	on	off
on	on	on	on	on	on
off	off	off	off	off	off

Whenever the brake switch is on and no turn signal switches are on all lamps are on:

<b>L1</b>	<b>L2</b>	<b>L3</b>	<b>R3</b>	<b>R2</b>	<b>R1</b>
on	on	on	on	on	on

Whenever the emergency flasher switch is on and the brake switch and the turn switches are off the following lamp sequence is displayed repeatedly:

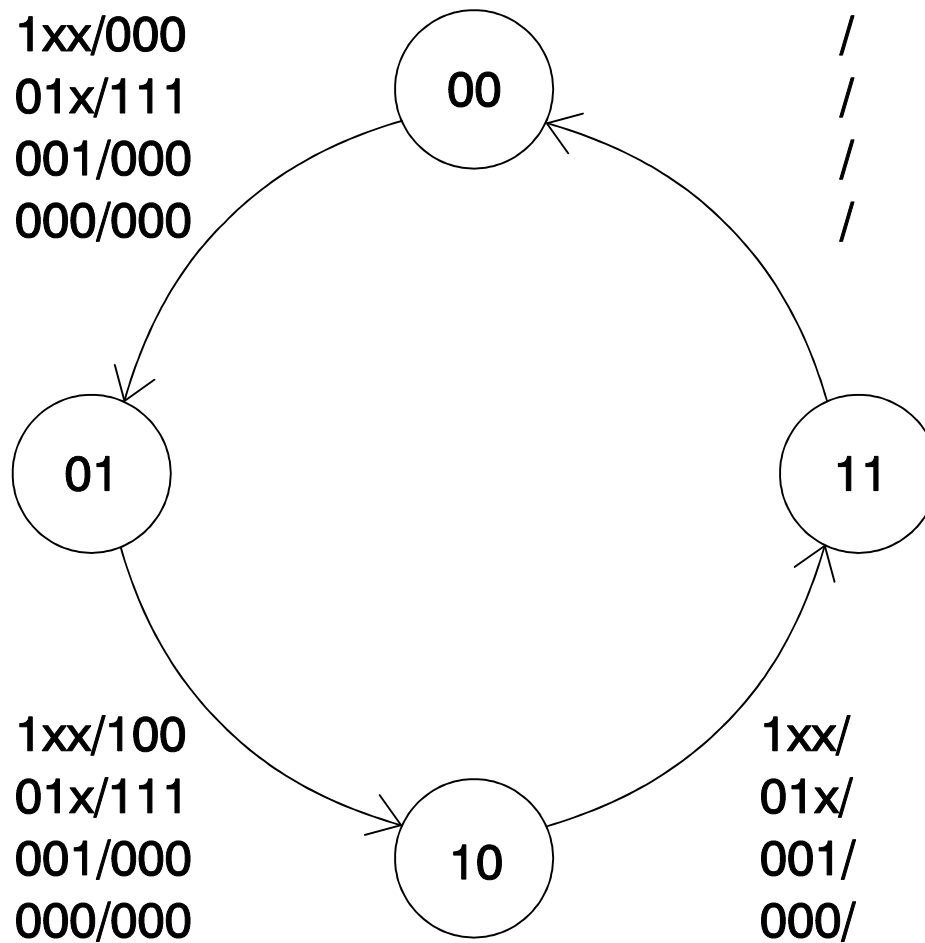
<b>L1</b>	<b>L2</b>	<b>L3</b>	<b>R3</b>	<b>R2</b>	<b>R1</b>
on	on	on	on	on	on
off	off	off	off	off	off

Whenever a turn signal switch is on, the turn signal sequence for that side is displayed regardless of the states of the brake switch or the emergency flasher switch. The other side is displayed normally. Whenever the brake switch is on and the turn signal switch is off, the brake lamps will be on regardless of the state of the emergency flasher switch.

Design and build the circuit for the **RIGHT SIDE ONLY**. Use a 555 oscillator circuit for the clock and 74LS112 or 74LS113 J-K flip-flops to hold the state of the system. Set the frequency of the 555 so that the turn signal sequence repeats approximately every 2 seconds. Show all work including the state diagram, state table, excitation table, and schematic.

**FOR YOUR BENEFIT:**

1. To get you started the following state diagram may be used. It has only been completed for two of the four transitions so you must fill in the rest. Optionally, you may design your own.
2. The five-variable blank Karnaugh maps may be used to save you the trouble of drawing your own. Be sure to circle the largest power of 2 number of 1s (or 0s) possible in each group and to consider mirrored squares adjacent.



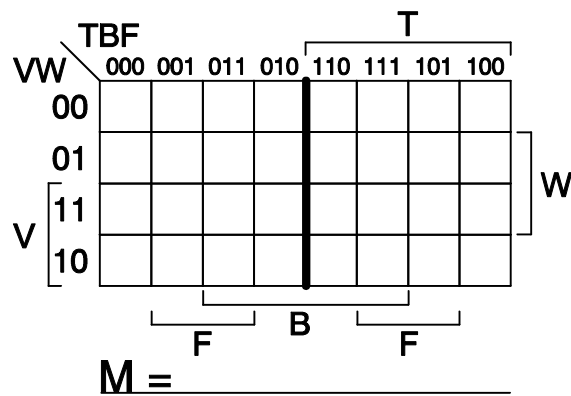
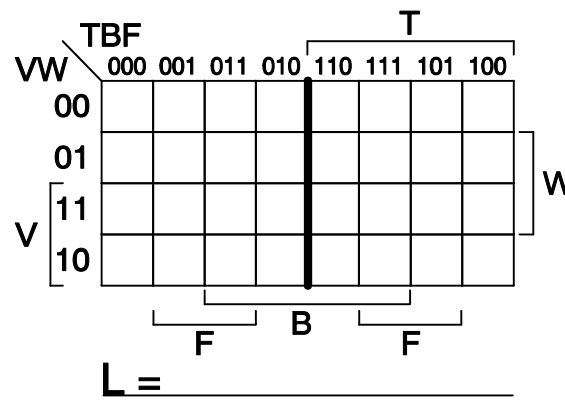
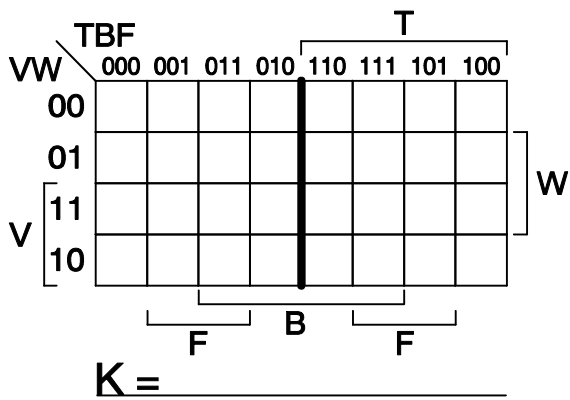
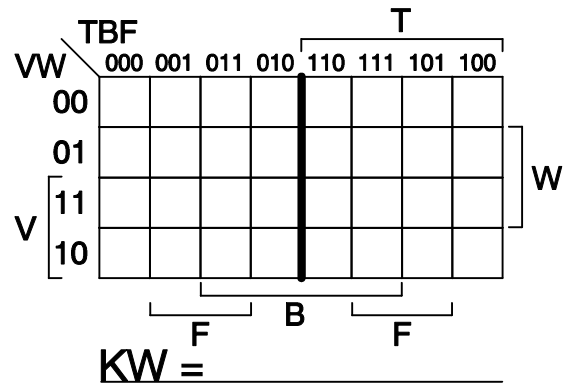
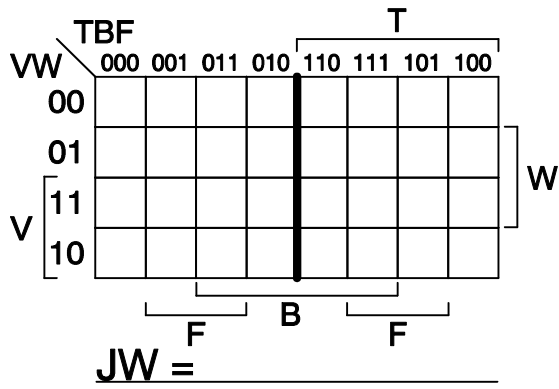
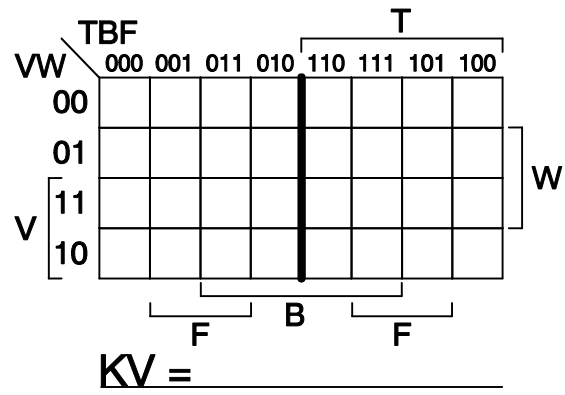
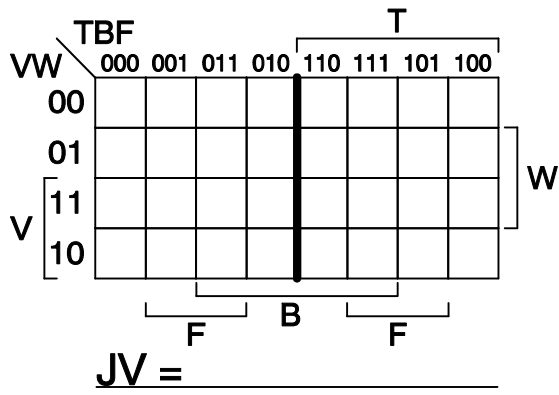
State Labels: VW where

V = Flip-flop V state (MSD)    1 => Set  
 W = Flip-flop W state (LSD)    1 => Set

Transition Labels: TBF / KLM where:

T = Turn;	1 => Asserted	K = LED R3;	1 => ON
B = Brake;	1 => Asserted	L = LED R2;	1 => ON
F = Flash;	1 => Asserted	M = LED R1;	1 => ON

### State Diagram For Sequential Turn Signal



**Karnaugh Maps For Sequential Turn Signal**

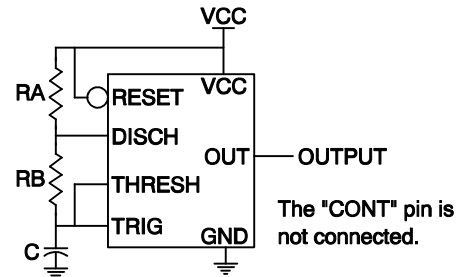
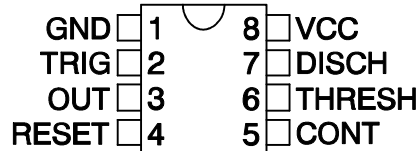
## Data Sheet: 555 Timer

The 555 is a monolithic timing circuit capable of producing accurate time delays or oscillation. In the time-delay or monostable mode of operation the timed interval is controlled by a single external resistor and capacitor network. In the astable mode of operation the frequency and duty cycle may be independently controlled with two external resistors and a single external capacitor.

The threshold and trigger levels are normally two-thirds and one-third, respectively, of  $V_{CC}$ . These levels can be altered by use of the control voltage terminal. When the trigger input falls below the trigger level the flip-flop is set and the output goes high. If the trigger input is above the trigger level and the threshold input is above the threshold level, the flip-flop is reset and the output is low. The reset input can override all other inputs and can be used to initiate a new timing cycle. When the reset input goes low the flip-flop is reset and the output goes low. Whenever the output is low, a low-impedance path is provided between the discharge terminal and ground.

The output circuit is capable of sinking or sourcing current up to 200 milliamperes. Operation is specified for supplies of 5 to 15 volts. With a 5-volt supply output levels are compatible with TTL inputs.

### DUAL-IN-LINE PACKAGE (TOP VIEW)

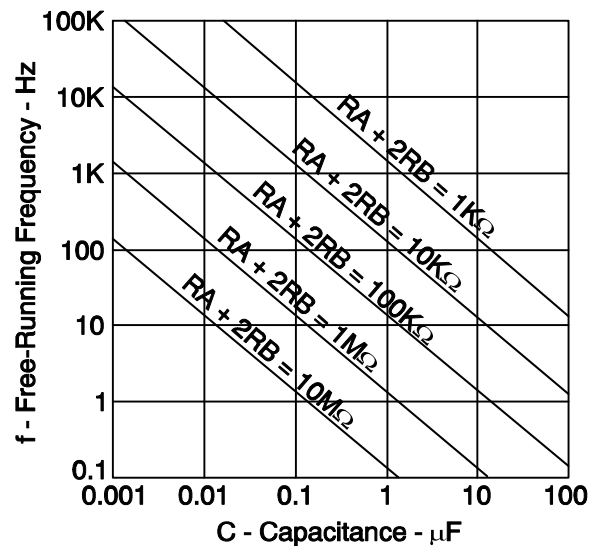


$$t_H = 0.693 * (RA + RB) * C$$

$$t_L = 0.693 * RB * C$$

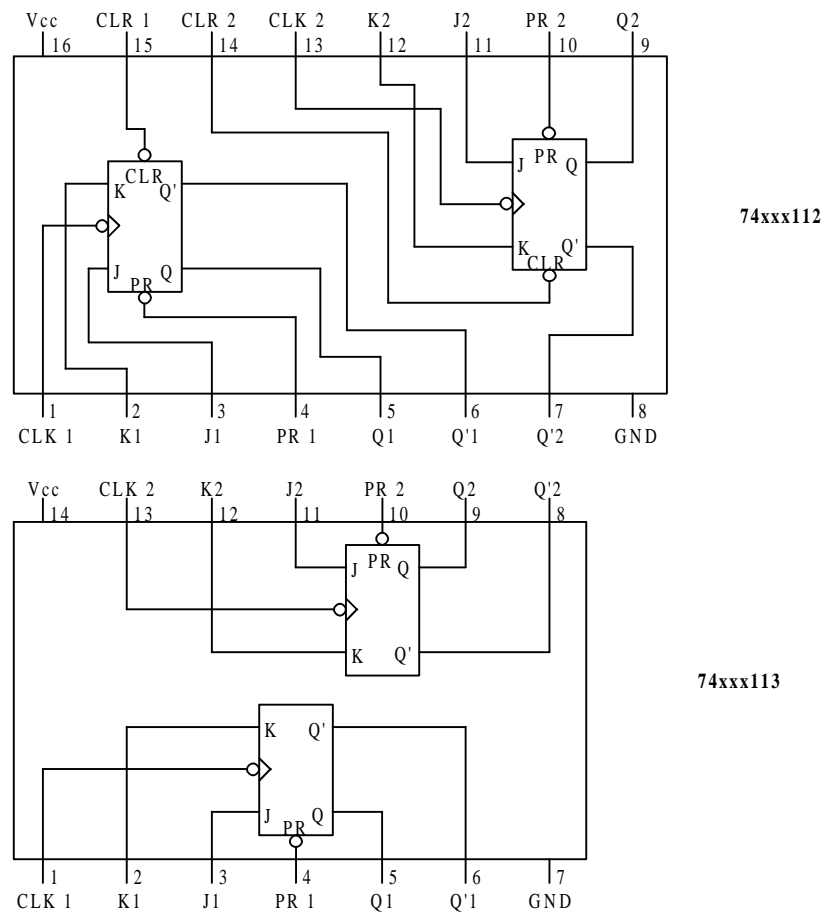
$$\text{period} = t_H + t_L = 0.693 * (RA + 2RB) * C$$

$$\text{frequency} = 1.44 / ((RA + 2RB) * C)$$



## Data Sheet: 74xxx112 and 74xxx113

The 74xxx112 and 74xxx113 are dual J-K negative-edge-triggered flip-flops. Each flip-flop has individual J, K, clock and preset inputs, along with complementary Q and Q' outputs. In addition each 74xxx112 flip-flop has individual clear inputs. Information at input J or K is transferred to the Q output on the negative going edge of the clock pulse. When the clock input is at either the high or low level, the J, K input signal has no effect. Asynchronous preset and clear inputs will set or clear the Q output respectively upon the application of the low level signal.

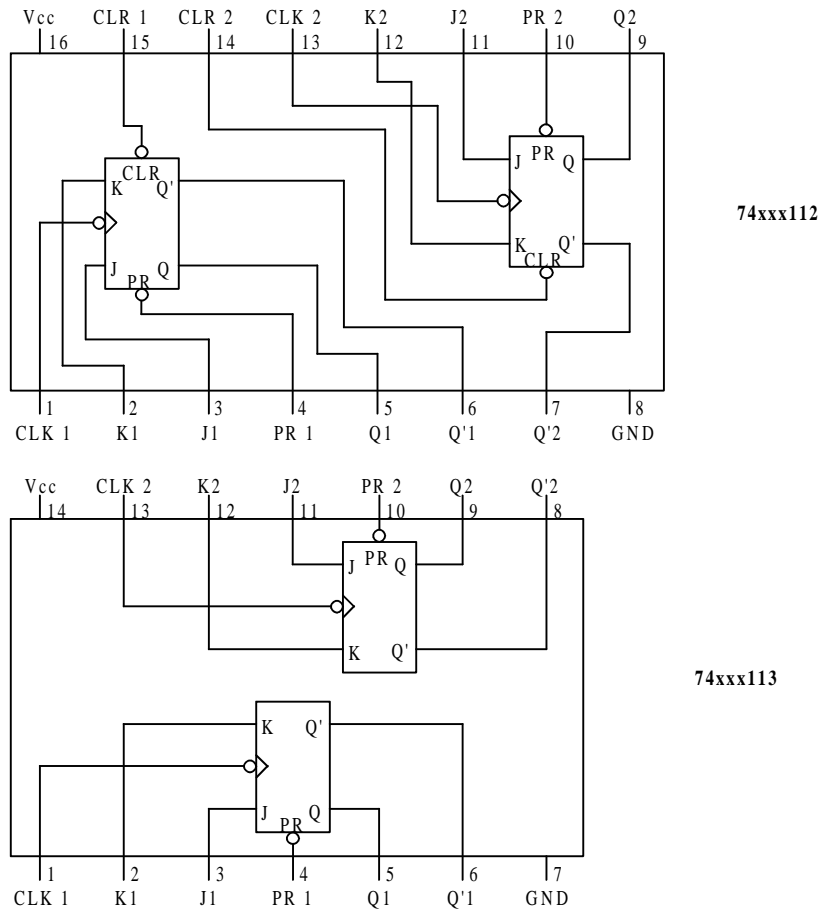


INPUTS					OUTPUTS	
PRESET	CLEAR	CLOCK	J	K	Q*	Q'*
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H <sup>1</sup>	H <sup>1</sup>
H	H	↓	L	L	Q	Q'
H	H	↓	H	L	H	L
H	H	↓	L	H	L	H
H	H	↓	H	H	TOGGLE	
H	H	H	X	X	Q	Q'

<sup>1</sup>This configuration is nonstable; that is, it will not persist when the preset and clear inputs return to their inactive (high) level.

### Data Sheet: 74xxx112 and 74xxx113

The 74xxx112 and 74xxx113 are dual J-K negative-edge-triggered flip-flops. Each flip-flop has individual J, K, clock and preset inputs, along with complementary Q and Q' outputs. In addition each 74xxx112 flip-flop has individual clear inputs. Information at input J or K is transferred to the Q output on the negative going edge of the clock pulse. When the clock input is at either the high or low level, the J, K input signal has no effect. Asynchronous preset and clear inputs will set or clear the Q output respectively upon the application of the low level signal.



INPUTS					OUTPUTS	
PRESET	CLEAR	CLOCK	J	K	Q*	Q'*
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H <sup>1</sup>	H <sup>1</sup>
H	H	↓	L	L	Q	Q'
H	H	↓	H	L	H	L
H	H	↓	L	H	L	H
H	H	↓	H	H	TOGGLE	
H	H	H	X	X	Q	Q'

<sup>1</sup>This configuration is nonstable; that is, it will not persist when the preset and clear inputs return to their inactive (high) level.

