

Interface Definition of Terms and Glossary

Definition of Terms

DC Characteristics

Currents:	Positive current is defined as conventional current flow into a device. Negative current is defined as current flow out of a device.	V_{CCQ}	Supply voltage used for internal circuitry requiring less noise.
Voltages:	All voltages are referenced to the ground pin.	V_{IH}	Input HIGH Voltage. The minimum input voltage that is recognized as a DC HIGH-level.
I_{CC}	The current flowing into the V _{CC} supply terminal when the device is at a quiescent state.	V_{IHD}	Dynamic Input HIGH Voltage. The minimum input voltage that is recognized as a HIGH-level during a Multiple Output Switching (MOS) operation.
I_{CCH}	The current flowing into the V _{CC} supply terminal when the outputs are in the HIGH state.	V_{IL}	Input LOW Voltage. The maximum input voltage that is recognized as a DC LOW-level.
I_{CCL}	The current flowing into the V _{CC} supply terminal when the outputs are in the LOW state.	V_{ILD}	Dynamic Input LOW Voltage. The maximum input voltage that is recognized as a LOW-level during Multiple Output Switching (MOS) operation.
I_{CCT}	See ΔI_{CC} definition.	V_{IK}	Input Clamp Diode Voltage. The voltage on an input when a specified current is pulled from that input.
I_{CCZ}	The current flowing into the V _{CC} supply terminal when the outputs are disabled (high impedance).	V_{OH}	Output HIGH Voltage. The voltage at an output conditioned HIGH with a specified output load and V _{CC} supply voltage.
I_I, I_{IN}	Input Current. The current flowing into or out of an input when a specified LOW or HIGH voltage is applied to that input.	V_{OL}	Output LOW Voltage. The voltage at an output conditioned LOW with a specified output load and V _{CC} supply voltage.
I_{OH}	Output HIGH Current. The current flowing out of an output which is in the HIGH state.	V_{OLP}	Maximum (peak) voltage induced on a static LOW output during switching of other outputs.
I_{I(HOLD)}	Input hold Current. Input current that holds the input at the previous state when the driving device goes to a high impedance state.	V_{OLV}	Minimum (valley) voltage induced on a static LOW output during switching of other outputs.
I_{I(OD)}	Input over-drive current. Input current that is specified to switch a logic level which is held at previous state.	V_{REF}	Voltage reference input used to reference the GTLP/GTL signal.
I_{OFF}	Input/Output power-off leakage current. The maximum leakage current into or out of the input/output transistors when forcing the input/output from 0V to 5.5V with V _{CC} = 0V.	V_{TT}	Termination voltage on the open drain outputs.
I_{OL}	Output LOW Current. The current flowing into an output which is in the LOW state.	ΔI_{CC}	Additional I _{CC} due to TTL HIGH levels forced on CMOS inputs.
I_{OS}	Output Short Circuit Current. The current flowing out of an output in the HIGH state when that output is shorted to ground (or other specified potential).	ΔV_T or Hysteresis	The difference between a positive-going and negative-going input threshold.
I_{OZ}	Output OFF current. The current flowing into or out of a disabled 3-STATE output when a specified LOW or HIGH voltage is applied to that output.		
I_{PU/PD}	The current flowing into or out of an output during power up or power down of the device. Applies to devices with live insertion feature only.		
R_{ON}	Switch on resistance. Applies to switch family only.		
V_{CC}	Supply Voltage. The range of power supply voltages over which the device is guaranteed to operate.		

Definition of Terms (Continued)

AC Characteristics

f_t	Maximum Transistor Operating Frequency —The frequency at which the gain of the transistor has dropped by three decibels.	t_{PZH}	Output Enable Time (of a 3-STATE Output) to a HIGH Level — The time between the specified levels of the input and output voltage waveforms with the 3-STATE output changing from a high impedance (OFF) state to a HIGH level.
f_{CLOCK}	The maximum frequency or clock rate at which pulses may be applied to the clock pin of a device typically operating in the registered mode. Above this frequency the device may cease to function. This term is sometimes used synonymous with f_{MAX} .	t_{PZL}	Output Enable Time (of a 3-STATE Output) to a LOW Level — The time between the specified levels of the input and output voltage waveforms with the 3-STATE output changing from a high impedance (OFF) state to a LOW level.
f_{MAX}	Toggle Frequency/Operating Frequency. The maximum rate at which clock pulses may be applied to a sequential circuit. Above this frequency the device may cease to function.	t_{rec}	Recovery Time — The time between the specified level on the trailing edge of an asynchronous input control pulse and the same level on a synchronous input (clock) pulse such that the device will respond to the synchronous input.
f_{TOGGLE}	The maximum frequency at which pulses may be applied to the data pin of a device typically operating in the transparent mode. Above this frequency the device may cease to function. This term is sometimes used synonymous with f_{MAX} .	t_{RISE}	Rise Time — Output transition time from LOW state to HIGH state.
t_{FALL}	Fall Time — Output transition time from HIGH state to LOW state.	t_S	Setup Time — The interval immediately preceding the active transition of the timing pulse (usually the clock pulse) or preceding the transition of the control input to its latching level, during which interval the data to be recognized must be maintained at the input to ensure its recognition. A negative setup time indicates that the correct logic level may be initiated sometime after the active transition of the timing pulse and still be recognized.
t_H	Hold Time — The interval immediately following the active transition of the timing pulse (usually the clock pulse) or following the transition of the control input to its latching level, during which interval the data to be recognized must be maintained at the input to ensure its continued recognition. A negative hold time indicates that the correct logic level may be released prior to the active transition of the timing pulse and still be recognized.	t_{THL}	Fall Time — Output transition time from HIGH state to LOW state.
t_{OSHL}	Output Skew — Output Skew for HIGH-to-LOW transitions. (See Note)	t_{TLH}	Rise Time — Output transition time from LOW state to HIGH state.
t_{OSLH}	Output Skew — Output Skew for LOW-to-HIGH transitions. (See Note)	t_W	Pulse Width — The time between specified amplitude points of the leading and trailing edges of a pulse.
t_{PHL}	Propagation Delay Time — The time between the specified reference points, on the input and output voltage waveforms, with the output changing from the defined HIGH level to the defined LOW level.	Note: More information regarding skew testing and definitions can be found later in this section.	
t_{PHZ}	Output Disable Time (of a 3-STATE Output) from HIGH Level — The time between specified levels on the input and a voltage 0.3V below the steady state output HIGH level with the 3-STATE output changing from the defined HIGH level to a high impedance (OFF) state.	Capacitance	
t_{PLH}	Propagation Delay Time — The time between the specified reference points, on the input and output voltage waveforms, with the output changing from the defined LOW level to the defined HIGH level.	C_{IN}	Input Capacitance
t_{PLZ}	Output Disable Time (of a 3-STATE Output) from LOW Level — The time between specified levels on the input and a voltage 0.3V above the steady state output LOW level with the 3-STATE output changing from the defined LOW level to a high impedance (OFF) state.	$C_{I/O}$	Input/Output Capacitance
		C_{OUT}	Output Capacitance
		C_{PD}	Power Dissipation Capacitance

DM74ALS04B Hex Inverter

General Description

This device contains six independent gates, each of which performs the logic INVERT function.

Features

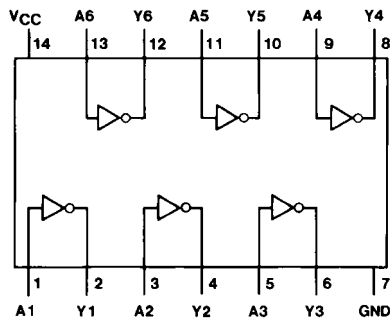
- Switching specifications at 50 pF
- Switching specifications guaranteed over full temperature and V_{CC} range
- Advanced oxide-isolated, ion-implanted Schottky TTL process
- Functionally and pin for pin compatible with Schottky and low power Schottky TTL counterpart
- Improved AC performance over Schottky and low power Schottky counterparts

Ordering Code:

Order Number	Package Number	Package Description
DM74ALS04BM	M14A	14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150 Narrow
DM74ALS04BSJ	M14D	14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
DM74ALS04BN	N14A	14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Connection Diagram



Function Table

$$Y = \bar{A}$$

Input	Output
A	Y
L	H
H	L

H = HIGH Logic Level
L = LOW Logic Level

Absolute Maximum Ratings(Note 1)

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	0°C to +70°C
Storage Temperature Range	-65°C to +150°C
Typical θ_{JA}	
N Package	88.0°C/W
M Package	118.5°C/W

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Recommended Operating Conditions

Symbol	Parameter	Min	Nom	Max	Units
V_{CC}	Supply Voltage	4.5	5	5.5	V
V_{IH}	HIGH Level Input Voltage	2			V
V_{IL}	LOW Level Input Voltage			0.8	V
I_{OH}	HIGH Level Output Current			-0.4	mA
I_{OL}	LOW Level Output Current			8	mA
T_A	Free Air Operating Temperature	0		70	°C

Electrical Characteristics

over recommended operating free air temperature range. All typical values are measured at $V_{CC} = 5V$, $T_A = 25^\circ C$.

Symbol	Parameter	Conditions		Min	Typ	Max	Units
V_{IK}	Input Clamp Voltage	$V_{CC} = 4.5V$, $I_I = -18\text{ mA}$				-1.2	V
V_{OH}	HIGH Level Output Voltage	$I_{OH} = -0.4\text{ mA}$ $V_{CC} = 4.5V\text{ to }5.5V$		$V_{CC} - 2$			V
V_{OL}	LOW Level Output Voltage	$V_{CC} = 4.5V$	$I_{OL} = 8\text{ mA}$		0.35	0.5	V
I_I	Input Current @ Maximum Input Voltage	$V_{CC} = 5.5V$, $V_{IH} = 7V$				0.1	mA
I_{IH}	HIGH Level Input Current	$V_{CC} = 5.5V$, $V_{IH} = 2.7V$				20	μA
I_{IL}	LOW Level Input Current	$V_{CC} = 5.5V$, $V_{IL} = 0.4V$				-0.1	mA
I_O	Output Drive Current	$V_{CC} = 5.5V$	$V_O = 2.25V$	-30		-112	mA
I_{CC}	Supply Current	$V_{CC} = 5.5V$	Outputs HIGH		0.65	1.1	mA
			Outputs LOW		2.4	4.2	mA

Switching Characteristics

over recommended operating free air temperature range

Symbol	Parameter	Conditions	Min	Max	Units
t_{PLH}	Propagation Delay Time LOW-to-HIGH Level Output	$V_{CC} = 4.5V\text{ to }5.5V$ $R_L = 500\Omega$	3	11	ns
t_{PHL}	Propagation Delay Time HIGH-to-LOW Level Output	$C_L = 50\text{ pF}$	2	8	ns

DM74AS04 Hex Inverter

General Description

This device contains six independent gates, each of which performs the logic INVERT function.

Features

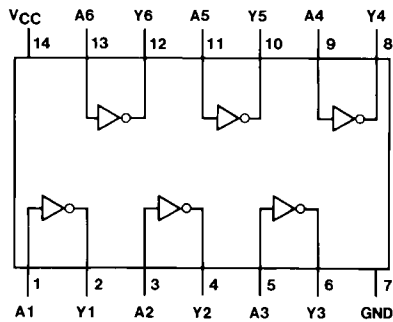
- Switching specifications at 50 pF
- Switching specifications guaranteed over full temperature and V_{CC} range
- Advanced oxide-isolated, ion-implanted Schottky TTL process
- Functionally and pin for pin compatible with Schottky and low power Schottky TTL counterpart
- Improved AC performance over Schottky and low power Schottky counterparts

Ordering Code:

Order Number	Package Number	Package Description
DM74AS04M	M14A	14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150 Narrow
DM74AS04SJ	M14D	14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
DM74AS04N	N14A	14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Connection Diagram



Function Table

$$Y = \bar{A}$$

Input A	Output Y
L	H
H	L

H = HIGH Logic Level
L = LOW Logic Level

Absolute Maximum Ratings(Note 1)

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	0°C to +70°C
Storage Temperature Range	-65°C to +150°C
Typical θ_{JA}	
N Package	84.5°C/W
M Package	115.0°C/W

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Recommended Operating Conditions

Symbol	Parameter	Min	Nom	Max	Units
V_{CC}	Supply Voltage	4.5	5	5.5	V
V_{IH}	HIGH Level Input Voltage	2			V
V_{IL}	LOW Level Input Voltage			0.8	V
I_{OH}	HIGH Level Output Current			-2	mA
I_{OL}	LOW Level Output Current			20	mA
T_A	Free Air Operating Temperature	0		70	°C

Electrical Characteristics

over recommended operating free air temperature range. All typical values are measured at $V_{CC} = 5V$, $T_A = 25^\circ C$.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{IK}	Input Clamp Voltage	$V_{CC} = 4.5V$, $I_I = -18\text{ mA}$			-1.2	V
V_{OH}	HIGH Level Output Voltage	$I_{OH} = -2\text{ mA}$ $V_{CC} = 4.5V\text{ to }5.5V$	$V_{CC} - 2$			V
V_{OL}	LOW Level Output Voltage	$V_{CC} = 4.5V$ $I_{OL} = 20\text{ mA}$		0.35	0.5	V
I_I	Input Current @ Max Input Voltage	$V_{CC} = 5.5V$, $V_{IH} = 7V$			0.1	mA
I_{IH}	HIGH Level Input Current	$V_{CC} = 5.5V$, $V_{IH} = 2.7V$			20	μA
I_{IL}	LOW Level Input Current	$V_{CC} = 5.5V$, $V_{IL} = 0.4V$			-0.5	mA
I_O	Output Drive Current	$V_{CC} = 5.5V$, $V_O = 2.25V$	-30		-112	mA
I_{CC}	Supply Current	$V_{CC} = 5.5V$				
		Outputs HIGH		3	4.8	mA
		Outputs LOW		14	26.3	mA

Switching Characteristics

over recommended operating free air temperature range

Symbol	Parameter	Conditions	Min	Max	Units
t_{PLH}	Propagation Delay Time LOW-to-HIGH Level Output	$V_{CC} = 4.5V\text{ to }5.5V$ $R_L = 500\Omega$	1	5	ns
t_{PHL}	Propagation Delay Time HIGH-to-LOW Level Output	$C_L = 50\text{ pF}$	1	4	ns

DM74ALS05A Hex Inverter with Open Collector Outputs

General Description

This device contains six independent gates, each of which performs the logic INVERT function. The open-collector outputs require external pull-up resistors for proper logical operation.

Pull-Up Resistor Equations

$$R_{MAX} = \frac{V_{CC} (Min) - V_{OH}}{N_1 (I_{OH}) + N_2 (I_{IH})}$$

$$R_{MIN} = \frac{V_{CC} (Max) - V_{OL}}{I_{OL} - N_3 (I_{IL})}$$

Where: $N_1 (I_{OH})$ = total maximum output HIGH current for all outputs tied to pull-up resistor
 $N_2 (I_{IH})$ = total maximum input HIGH current for all inputs tied to pull-up resistor
 $N_3 (I_{IL})$ = total maximum input LOW current for all inputs tied to pull-up resistor

Features

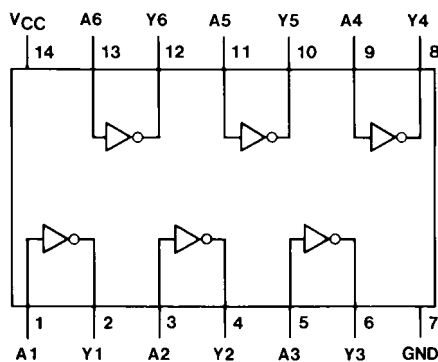
- Switching specifications at 50 pF
- Switching specifications guaranteed over full temperature and V_{CC} range
- Advanced oxide-isolated, ion-implanted Schottky TTL process
- Functionally and pin for pin compatible with Schottky and low power Schottky TTL counterpart
- Improved AC performance over Schottky and low power Schottky counterparts

Ordering Code:

Order Number	Package Number	Package Description
DM74ALS05AM	M14A	14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150 Narrow
DM74ALS05AN	N14A	14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Connection Diagram



Function Table

$$Y = \bar{A}$$

Input	Output
A	Y
L	H
H	L

H = HIGH Logic Level
L = LOW Logic Level

Absolute Maximum Ratings(Note 1)

Supply Voltage	7V
Input Voltage	7V
HIGH Level Output Voltage	7V
Operating Free Air Temperature Range	0°C to +70°C
Storage Temperature Range	-65°C to +150°C
Typical θ_{JA}	
N Package	88.0°C/W
M Package	118.5°C/W

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Recommended Operating Conditions

Symbol	Parameter	Min	Nom	Max	Units
V_{CC}	Supply Voltage	4.5	5	5.5	V
V_{IH}	HIGH Level Input Voltage	2			V
V_{IL}	LOW Level Input Voltage			0.8	V
V_{OH}	HIGH Level Output Voltage			5.5	V
I_{OL}	LOW Level Output Current			8	mA
T_A	Free Air Operating Temperature	0		70	°C

Electrical Characteristics

over recommended operating free air temperature range. All typical values are measured at $V_{CC} = 5V$, $T_A = 25^\circ C$.

Symbol	Parameter	Conditions	Min	Typ	Max	Units	
V_{IK}	Input Clamp Voltage	$V_{CC} = 4.5V$, $I_I = -18\text{ mA}$			-1.5	V	
I_{OH}	HIGH Level Output Current	$V_{CC} = 4.5V$, $V_{OH} = 5.5V$			100	μA	
V_{OL}	LOW Level Output Voltage	$V_{CC} = 4.5V$	$I_{OL} = 4\text{ mA}$		0.25	0.4	V
			$I_{OL} = 8\text{ mA}$		0.35	0.5	V
I_I	Input Current @ Max Input Voltage	$V_{CC} = 5.5V$, $V_{IH} = 7V$			0.1	mA	
I_{IH}	HIGH Level Input Current	$V_{CC} = 5.5V$, $V_{IH} = 2.7V$			20	μA	
I_{IL}	LOW Level Input Current	$V_{CC} = 5.5V$, $V_{IL} = 0.4V$			-0.1	mA	
I_{CC}	Supply Current	$V_{CC} = 5.5V$	Outputs HIGH		0.65	1.1	mA
			Outputs LOW		2.4	4.2	mA

Switching Characteristics

over recommended operating free air temperature range

Symbol	Parameter	Conditions	Min	Max	Units
t_{PLH}	Propagation Delay Time	$V_{CC} = 4.5V$ to $5.5V$ $R_L = 2\text{ k}\Omega$, $C_L = 50\text{ pF}$	23	54	ns
	LOW-to-HIGH Level Output				
t_{PHL}	Propagation Delay Time		4	14	ns
	HIGH-to-LOW Level Output				

DM74ALS374

Octal 3-STATE D-Type Edge-Triggered Flip-Flop

General Description

This 8-bit register features totem-pole 3-STATE outputs designed specifically for driving highly-capacitive or relatively low-impedance loads. The high-impedance state and increased high-logic-level drive provides this register with the capability of being connected directly to and driving the bus lines in a bus-organized system without need for interface or pull-up components. It is particularly attractive for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The eight flip-flops of the DM74ALS374 are edge-triggered D-type flip-flops. On the positive transition of the clock, the Q outputs will be set to the logic states that were set up at the D inputs.

A buffered output control input can be used to place the eight outputs in either a normal logic state (HIGH or LOW logic levels) or a high-impedance state. In the high-impedance state the outputs neither load nor drive the bus lines significantly.

The output control does not affect the internal operation of the flip-flops. That is, the old data can be retained or new data can be entered even while the outputs are OFF.

Features

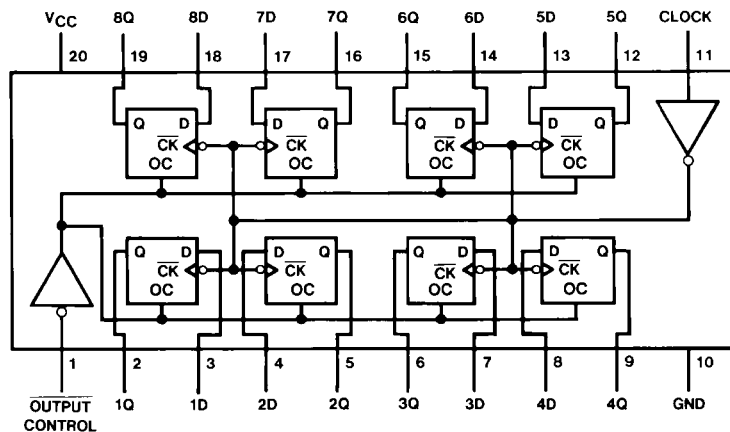
- Switching specifications at 50 pF
- Switching specifications guaranteed over full temperature and V_{CC} range
- Advanced oxide-isolated, ion-implanted Schottky TTL process
- Functionally and pin-for-pin compatible with LS TTL counterpart
- Improved AC performance over DM74LS374 at approximately half the power
- 3-STATE buffer-type outputs drive bus lines directly

Ordering Code:

Order Number	Package Number	Package Description
DM74ALS374WM	M20B	20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300 Wide
DM74ALS374SJ	M20D	20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
DM74ALS374N	N20A	20-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide

Device also available in Tape and Reel. Specify by appending suffix letter "X" to the ordering code.

Connection Diagram

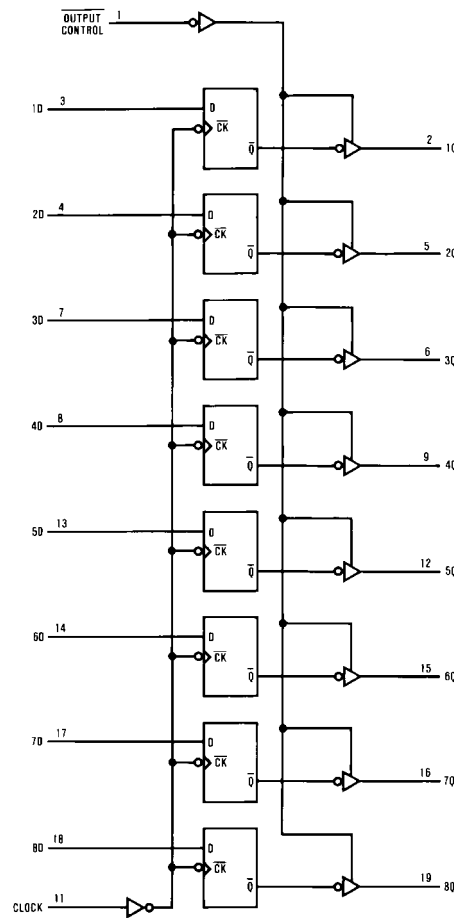


Function Table

Output Control	Clock	D	Output Q
L	↑	H	H
L	↑	L	L
L	L	X	Q ₀
H	X	X	Z

L = LOW State
 H = HIGH State
 X = Don't Care
 ↑ = Positive Edge Transition
 Z = High Impedance State
 Q₀ = Previous Condition of Q

Logic Diagram



Absolute Maximum Ratings(Note 1)

Supply Voltage	7V
Input Voltage	7V
Voltage Applied to Disabled Output	5.5V
Operating Free Air Temperature Range	0°C to +70°C
Storage Temperature Range (Note 2)	-65°C to +150°C
Typical θ_{JA}	
N Package	60.0°C/W
M Package	79.0°C/W

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Note 2: This product meets application requirements of 500 temperature cycles from -65°C to +150°C.

Recommended Operating Conditions

Symbol	Parameter	Min	Nom	Max	Units
V_{CC}	Supply Voltage	4.5	5	5.5	V
V_{IH}	HIGH Level Input Voltage	2			V
V_{IL}	LOW Level Input Voltage			0.8	V
I_{OH}	HIGH Level Output Current			-2.6	mA
I_{OL}	LOW Level Output Current			24	mA
f_{CLOCK}	Clock Frequency	0		35	MHz
t_W	Width of Clock Pulse	HIGH	14		ns
		LOW	14		ns
t_{SU}	Data Setup Time (Note 3)	10 \uparrow			ns
t_H	Data Hold Time (Note 3)	0 \uparrow			ns
T_A	Free Air Operating Temperature	0		70	°C

Note 3: The (1) arrow indicates the positive edge of the Clock is used for reference.

DC Electrical Characteristics

over recommended operating free air temperature range. All typical values are measured at $V_{CC} = 5V$, $T_A = 25^\circ C$.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{IK}	Input Clamp Voltage	$V_{CC} = 4.5V$, $I_I = -18 mA$			-1.5	V
V_{OH}	HIGH Level Output Voltage	$V_{CC} = 4.5V$	$I_{OH} = \text{Max}$	2.4	3.2	V
		$V_{CC} = 4.5V$ to $5.5V$	$I_{OH} = -400 \mu A$	$V_{CC} - 2$		V
V_{OL}	LOW Level Output Voltage	$V_{CC} = 4.5V$	$I_{OL} = 12 mA$	0.25	0.4	V
			$I_{OL} = 24 mA$	0.35	0.5	V
I_I	Input Current @ Max. Input Voltage	$V_{CC} = 5.5V$, $V_{IH} = 7V$			0.1	mA
I_{IH}	HIGH Level Input Current	$V_{CC} = 5.5V$, $V_{IH} = 2.7V$			20	μA
I_{IL}	LOW Level Input Current	$V_{CC} = 5.5V$, $V_{IL} = 0.4V$			-0.2	mA
I_O	Output Drive Current	$V_{CC} = 5.5V$, $V_O = 2.25V$	-30		-112	mA
I_{OZH}	OFF-State Output Current, HIGH Level Voltage Applied	$V_{CC} = 5.5V$, $V_O = 2.7V$			20	μA
I_{OZL}	OFF-State Output Current, LOW Level Voltage Applied	$V_{CC} = 5.5V$, $V_O = 0.4V$			-20	μA
I_{CC}	Supply Current	$V_{CC} = 5.5V$ Outputs Open	Outputs HIGH	11	19	mA
			Outputs LOW	19	28	mA
			Outputs Disabled	20	31	mA

AC Electrical Characteristics

Symbol	Parameter	Conditions	From	To	Min	Max	Units
f_{MAX}	Maximum Clock Frequency	$V_{CC} = 4.5V$ to $5.5V$			35		MHz
t_{PLH}	Propagation Delay Time LOW-to-HIGH Level Output	$R_L = 500\Omega$ $C_L = 50$ pF	Clock	Any Q	3	12	ns
t_{PHL}	Propagation Delay Time HIGH-to-LOW Level Output		Clock	Any Q	5	16	ns
t_{PZH}	Output Enable Time to HIGH Level Output		Output Control	Any Q	5	17	ns
t_{PZL}	Output Enable Time to LOW Level Output		Output Control	Any Q	7	18	ns
t_{PHZ}	Output Disable Time from HIGH Level Output		Output Control	Any Q	2	10	ns
t_{PLZ}	Output Disable Time from LOW Level Output		Output Control	Any Q	3	18	ns